1300 V Normally-OFF p-GaN Gate HEMTs on Si With High ON-State Drain Current

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***Abstract*— In this article, we demonstrate normally-OFF p-GaN gate high electron mobility transistors (HEMTs) on Si with an ultrahigh breakdown voltage (V_{BR}) and excellent saturation drain current. Benefiting from the optimized material growth of high-resistivity buffer, effective Al_2O_3 surface passivation with suppressed OFF-state leakage current, and proper management of the electric field on the p-GaN gate edge, the device with a gate–drain distance of 18.5 μm exhibits a V_{BR} of 1344 V at I_D of 1 μA/mm with grounded substrates, the highest among all the reported normally-OFF GaN-on-Si transistors. Well-restored high-density 2-D electron gas and efficient gate modulation enable the device with a high $I_{DS,max}$ of 450 mA/mm and a low specific ON-resistance of 3.92 mΩ·cm^2. Moreover, a large threshold voltage of 1.6 V (at I_D of 10 μA/mm) and a steep subthreshold slope of 66 mV/dec have been achieved, with negligible threshold voltage shift upon long-term forward gate stress at 150 °C. These results illustrate the great potential of p-GaN gate HEMTs on Si for beyond 600-V applications.**

***Index Terms*— Breakdown voltage, GaN-on-Si, normally-OFF, p-GaN gate high electron mobility transistors (HEMTs).**

I. Introduction

TREMENDOUS progress has been made in the development of high-performance normally-OFF GaN high electron mobility transistors (HEMTs) over the past decade [1]–[14]. Among all the typical approaches including gate recess (thin barrier heterostructure), p-(Al)GaN gate, and fluorine implantation to realize positive threshold voltage (V_{th}) in the GaN transistors, the p-(Al)GaN gate HEMTs on Si stand out as the most cost-effective technology for rapid commercialization. To fully exploit the potential of the p-GaN gate HEMTs, enhanced OFF-state blocking capability and reduced ON-state power consumption are always desired device merits. However, to date, achieving a high breakdown voltage (V_{BR}) over 1300 V at a low leakage current of 1 μA/mm while maintaining an ON-resistance (R_{ON}) $\leq$ 15 Ω·mm at the same time is still challenging in this type of devices. This is mainly because (i) the thin AlGaN barrier in the heterostructure leaves little margin for the p-GaN etching depth control, thus undermining the 2-D electron gas (2-DEG) restoration in the access regions [15]; (ii) dielectric passivation on the etching-exposed AlGaN barrier could be a liability due to an extra possible leakage path through the dielectric/barrier (p-GaN sidewall) interface [16]; and (iii) last but not least, the epitaxy of p-GaN gate HEMTs on Si with a high-resistivity buffer and a well-controlled p-GaN doping profile still calls for continuous improvement, especially on large-scale Si substrates [17]. Many researchers have been tackling the above challenges from various perspectives. For instance, Zhong *et al.* [18] employed a regrown p-GaN gate process combining a low-pressure chemical vapor deposited SiN passivation to achieve a high $I_{DS,max}$. Hao *et al.* [19] used a hydrogen-plasma process to enhance the V_{BR}. Zhou *et al.* [20] and Stockman *et al.* [21] adopted special treatments in the gate-stack and p-GaN sidewall passivation, respectively, to suppress the gate leakage current. Nevertheless, attaining all these excellent device parameters in the same device is rarely reported.

In this article, we demonstrate high-performance p-GaN gate HEMTs grown on silicon substrates. The device with a gate–drain distance of 18.5 μm exhibits a high soft V_{BR} of 1344 V at I_D of 1 μA/mm with a grounded substrate, while maintains a low specific ON-resistance ($R_{ON,sp}$) of 3.92 mΩ·cm^2 and a high $I_{DS,max}$of 450 mA/mm, resulting in a high Baliga's figure of merit (BFOM = $V_{BR}^2/R_{ON,sp}$) of 461 MW/cm^2. Simultaneously, the device shows a large threshold voltage (V_{th}) of 1.6 V defined at I_D of 10 μA/mm, a nearly ideal subthreshold slope (*SS*) of 66 mV/dec, and negligible threshold voltage shift upon a 100 00-s forward gate stress of up to 8 V at both room temperature and 150 °C.

II. Device Design and Fabrication

The p-GaN/AlGaN/GaN heterostructure was grown on a 6-in Si substrate using metal organic chemical vapor deposition (MOCVD) [Fig. 1(a)]. The epilayers feature a 5-μm buffer, a 400-nm undoped GaN channel, a 10-nm $Al_{0.2}Ga_{0.8}N$ barrier, and a 70-nm p-GaN cap with a hole concentration

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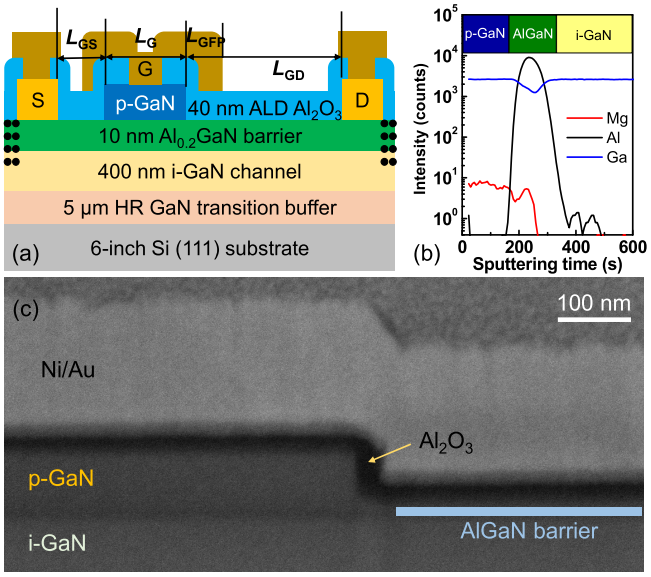

Fig. 1. (a) Cross-sectional schematic of a fabricated p-GaN HEMT. (b) Depth-profile SIMS measurement of Mg, Al, and Ga ions in the topmost layers of the epi structure. (c) Cross-sectional SEM image of the gate-stack near the p-GaN gate edge.

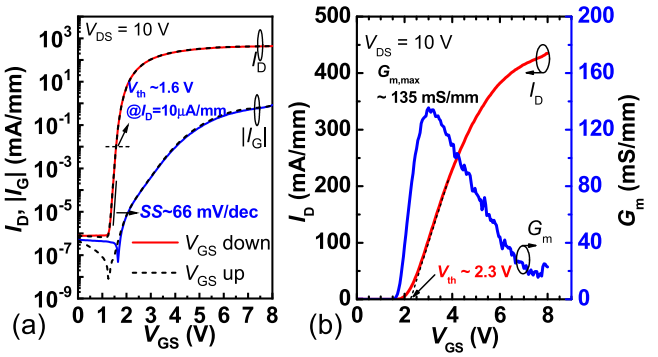

Fig. 2. Transfer characteristics of the p-GaN gate HEMTs plotted in (a) semi-log and (b) linear scale.

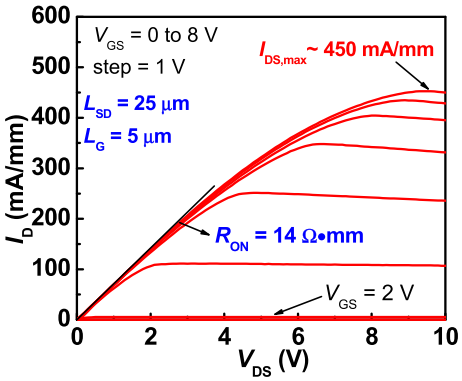

Fig. 3. Output characteristics of the p-GaN gate HEMT.

of $\sim 1 \times 10^{18}$ cm^{-3} after activation. Depth-profiling by secondary-ion mass spectrometry (SIMS) on the distribution of Al, Mg, and Ga elements in the topmost 500-nm layers of the as-grown sample [Fig. 1(b)] was carried out to investigate the diffusion of Mg dopants during the p-GaN growth and activation. It is evident that the Mg diffusion is well confined in the AlGaN barrier underneath the p-GaN, which is crucial to achieve a low R_{ON} and large V_{th} in the p-GaN gate HEMTs [22].

The device fabrication started with p-GaN gate patterning using a low-power (10 W) BCl_3/Cl_2-based inductively coupled plasma etching process to ensure a well-controlled etch stop at the AlGaN barrier surface, as shown in the cross-sectional scanning electron microscope (SEM) image [Fig. 1(c)]. Due to the low-power plasma process thus low physical ion bombardment, the exposed surface is almost as smooth as that of the as-grown sample as verified via atomic force microscopy measurement. The precise etch stop and smooth surface are critical to minimize 2-DEG concentration degradation in the access regions. The source–drain contacts were formed using an alloyed Ti/Al/Ni/Au-based metal stack and fluorine ion implantation was employed for planar device isolation. Then, the device was passivated with a 40-nm Al_2O_3 formed by atomic layer deposition (ALD) at 300 °C. After opening the contact holes on the p-GaN layer, a nonannealed Ni/Au metal stack was evaporated as the Schottky gate contact. Instead of using SiN for surface passivation as in our previous article [23], ALD Al_2O_3 passivation was chosen in this article because the ALD Al_2O_3 is likely to suppress the surface leakage current more effectively in the device than the plasma-enhanced chemical vapor deposited SiN [24]. Unless otherwise specified, the devices in this article feature a p-GaN gate length (L_G) of 5 μm, a gate–drain distance (L_{GD}) of 18.5 μm, a gate–source distance (L_{GS}) of 1.5 μm, and a gate width (W_G) of 10 μm. The gate metal foot is 2 μm, and the gate-connected field plate (GFP) is 2 μm on the drain side and 0.5 μm on the source side.

III. Device Results and Discussion

Fig. 2 shows the transfer characteristics of the fabricated device, exhibiting a respectably large V_{th} of 1.6 V defined at I_D of 10 μA/mm, or 2.3 V by linear extrapolation. Moreover, a high ON/OFF current ratio beyond 10^8 and a nearly ideal *SS* of 66 mV/dec, a high peak transconductance of 135 mS/mm are also achieved in the device, suggesting effective gate control over the channel. The gate leakage (I_G) remains as low as 1 mA/mm at a high V_{GS} of 8 V, thus enabling a large gate swing. The forward gate leakage could be further suppressed by increasing the Schottky barrier height with a low-work-function gate metal [25].

Facilitated by the carefully controlled p-GaN etching and effective Al_2O_3 passivation in the access regions as well as efficient gate modulation in the channel region, high-density 2-DEG are restored at the AlGaN/GaN heterointerface as the device turns on. As a result, a high driving current $I_{DS,max}$ of 450 mA/mm is achieved at V_{GS} of 8 V (Fig. 3). The R_{on} is extracted to be $\sim$14 Ω·mm, which corresponds to a specific ON-resistance $R_{on,sp}$ of 3.92 mΩ·cm^2, taking 1.5 μm transfer length for each Ohmic contact into account (each Ohmic contact resistance is $\sim$1 Ω·mm). Fig. 4 benchmarks the $I_{DS,max}$ versus V_{th} of the device in this article with reported

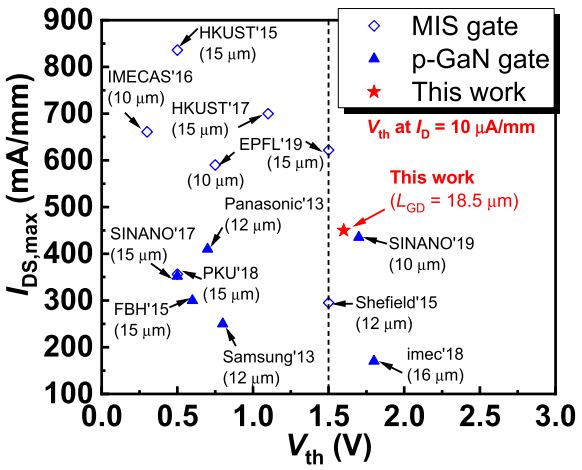

Fig. 4. Benchmarking of $I_{DS,max}$ versus V_{th} for state-of-the-art E-mode GaN transistors with MIS gates and p-GaN gates on Si. For fair comparison, only devices with $L_{GD} \geq 10$ μm are included here. The V_{th} is extracted from the transfer curves at I_D of 10 μA/mm in the literature.

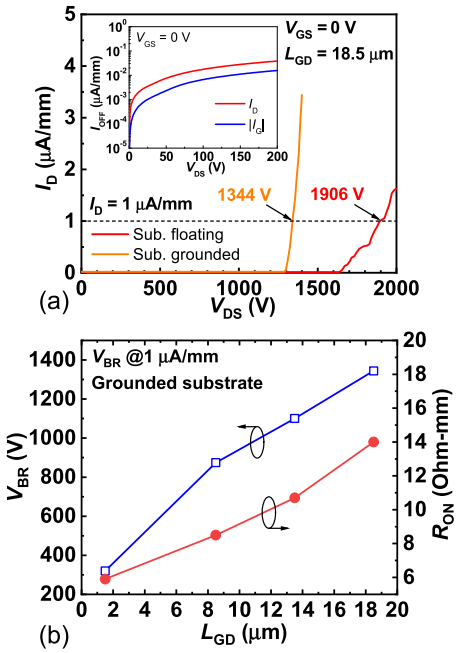

Fig. 5. (a) OFF-state I_D–V_{DS} of the p-GaN gate HEMTs. Inset: OFF-state I_D and I_G versus V_{DS} for $V_{DS} \leq 200$ V. (b) Dependence of V_{BR} and R_{ON} on the gate–drain distance L_{GD}.

state-of-the-art enhancement-mode GaN-on-Si HEMTs with either metal-insulator-semiconductor (MIS) gate structure or p-GaN gate structure. For a fair comparison, only devices with $L_{GD} \geq 10$ μm were included. It can be observed that most of the devices show a relatively small V_{th} (defined at I_D of 10 μA/mm) which is below 1.5 V. Our device not only shows a large V_{th} which provides more margin to prevent false turn-on, but also delivers a concurrently high $I_{DS,max}$ to enable efficient power conversion.

The soft OFF-state breakdown voltage of the device was measured with floating and grounded substrates at V_{GS} of 0 V, respectively [Fig. 5(a)]. With a floating substrate, the device shows a breakdown voltage of 1906 V at I_D of 1 μA/mm. The OFF-state I_D is still below 2 μA/mm at V_{DS} of 2000 V (the maximum bias of our equipment) with no sign of hard breakdown observed. The V_{BR} of the device with the substrate grounded is still as high as 1344 V, with the OFF-state I_D mainly arising from the substrate leakage current limited by the buffer resistivity. To our best knowledge, this is the highest value to date among all the reported normally-OFF GaN-on-Si transistors. Compared with the device (same dimensions) using SiN passivation in our previous article which has a typical V_{BR} of 1600 V with a floating substrate and 1160 V with a grounded substrate [23], the enhanced breakdown performance in this article suggests more effective suppression of leakage currents using Al_2O_3 passivation upon the high electric field stress. The dependence of breakdown voltage and ON-resistance on the gate–drain distance of the device is plotted in Fig. 5(b). It is clearly shown that increasing the drift length can enhance the voltage blocking capability effectively, at the price of greatly increased ON-resistance. Hence, trade-offs between V_{BR} and R_{ON} should be made in the device design in terms of different voltage rating applications. Benchmarked with normally-OFF GaN-on-Si transistors in the literature (Fig. 6), our device shows a remarkably high V_{BR} with a reasonable $R_{ON,sp}$, leading to an excellent BFOM of 461 MW/cm^2 (927 MW/cm^2) calculated with V_{BR} for grounded (floating) substrate, which suggests a good balance between OFF-state blocking capability and ON-state power loss. Nevertheless, compared with state-of-the-art nanostructured recessed normally-OFF GaN transistors [13], the R_{ON} in this article can still be further improved using other effective surface passivation and optimization on the barrier structure without sacrificing the breakdown performance. On the other hand, the dynamic resistance of the device was characterized by switching the device from high-voltage stressed OFF-state ($V_{GS} = 0$ V, V_{DS} ranges from 0 to 600 V) to ON-state ($V_{GS} = 7$ V). Due to the limit of the measurement equipment, the OFF-to-ON switching transient is around 1 s. To reveal the surface passivation effectiveness, the OFF-state stress is prolonged to be 10 s correspondingly to aggravate the trapping effect intentionally. The dynamic to static R_{ON} ratio is measured to be only around 1.8 after the OFF-state V_{DS} stress of 600 V, as shown in Fig. 7. The minimal increase in the R_{ON} after such long-term high-voltage stress still suggests the effective suppression of current collapse induced by slow traps in the device. The impact of traps with a short time constant (e.g., <1 ms) on the dynamic R_{ON} has been underestimated and should be evaluated by double-pulsed fast switching method to fully characterize the Al_2O_3 passivation effectiveness.

Threshold voltage stability is another important device metric in the p-GaN gate HEMTs with a Schottky gate metal. To evaluate the V_{th} stability in the device, large forward gate stress induced V_{th} shift (ΔV_{th}) was characterized at both room temperature (25 °C) and 150 °C. The stress measurement procedure was similar to that in our previous report for depletion-mode devices [26]. The device was submitted to a constant V_{GS} stress of 7, 8, and 9 V ($V_D = V_S = 0$ V), respectively, with a total stress time of 10 000 seconds for

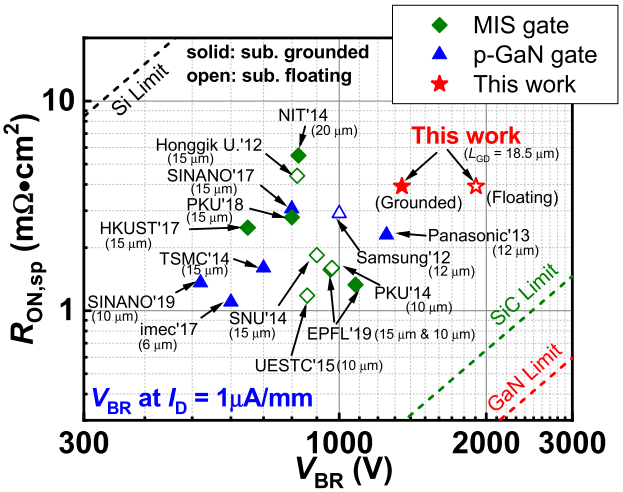

Fig. 6. Benchmarking of $R_{ON,sp}$ versus V_{BR} of the p-GaN gate HEMT in this article with other state-of-the-art normally-OFF GaN-on-Si transistors with MIS or p-GaN gate structures. Filled symbol: substrate grounded; open symbol: substrate floating. The V_{BR} is extracted at I_D of 1 μA/mm for the references.

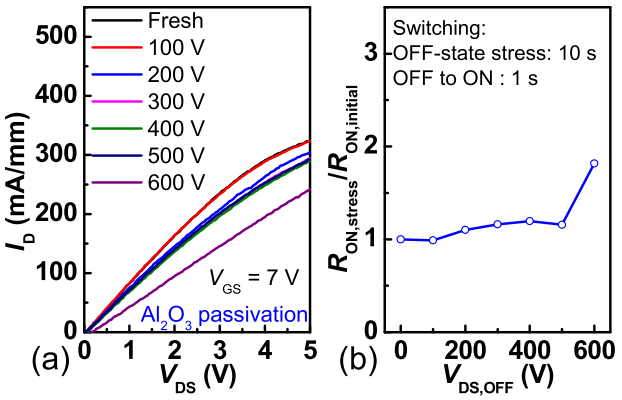

Fig. 7. (a) Output curves at V_{GS} of 7 V after various OFF-state V_{DS} stresses for 10 s. (b) Extracted dynamic to static R_{ON} ratio as a function of OFF-state V_{DS} bias.

each bias, and the V_{th} shift during the stress was monitored by a fast transfer curve measurement after certain stress time intervals (1, 3, 10, 30, 100, 300, 1000, 3000, and 10 000 s). The V_{th} is determined at I_D of 0.01 mA/mm. Fig. 8(a) and (b) show the transfer curves before and after the V_{GS} stress of 8 V at 25 °C and 150 °C, respectively. It can be seen that the device stressed at 25 °C shows much less severe degradation in the subthreshold characteristics but a slightly larger V_{th} shift than the device stressed at 150 °C. The V_{th} shift for each gate stress at 25 °C and 150 °C was plotted in Fig. 8(c) and (d), respectively, as a function of the stress time. The device shows a positive V_{th} shift of 0.2 V after the 10 000-s 9-V gate stress at 25 °C, while the gate of the device stressed at 150 °C was broken down during the 9-V stress interval between 1000 and 3000 s. Nevertheless, the V_{th} is nearly unchanged when the devices were stressed at 150 °C with $V_{GS,stress}$ of 7 and 8 V. The positive V_{th} shift suggests electron trapping (negative charge storage) in the gate-stack: upon large forward gate stress, the electrons from the 2-DEG channel may overcome the

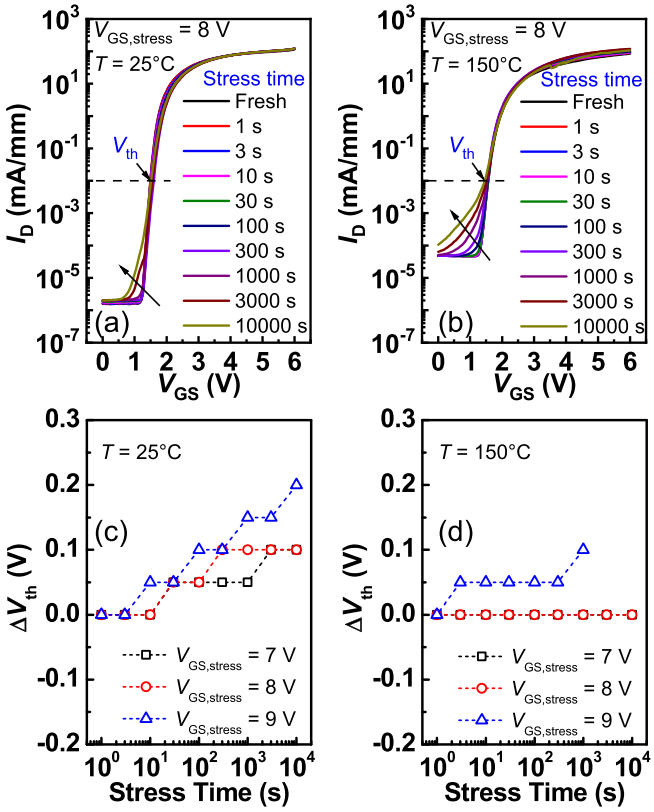

Fig. 8. Transfer characteristics of the p-GaN gate HEMTs during the 10000-s forward gate stress of 8 V at (a) 25 °C and (b) 150 °C. The extracted V_{th} shift as a function of stress time at $V_{GS,stress}$ of 7, 8, and 9 V at (c) 25 °C and (d) 150 °C.

AlGaN barrier and be trapped at the p-GaN/AlGaN interface or in the depleted p-GaN region. At elevated temperature, the trapped electrons may be thermally activated and quickly released from the trap states thus result in little influence on the device V_{th}. Therefore, the V_{th} shift at 150 °C is slightly smaller than that at 25 °C. The permanent degradation of the subthreshold characteristics of the stressed device may arise from the defects generated at the Schottky gate metal/p-GaN interface. Under the thermal stimulation at high temperature, defect generation is accelerated due to the high electric field across the reverse-biased Ni/p-GaN junction, where impact ionization may occur near the junction interface resulting in microscopic crystal destruction [27]–[32]. Consequently, the Ni/p-GaN Schottky contact is degraded thereby undermining the gate control over the channel. As a result, the device stressed at 150 °C showed much more severe degradation in the subthreshold characteristics than that at 25 °C. Nevertheless, the generated defects may remain charge-neutral during the gate stress, thus having little influence on the V_{th} shift. The comparison of device behaviors stressed at different temperatures suggests that the V_{th} shift and subthreshold characteristics degradation after the large forward gate stress are induced by different dominated trapping mechanisms. To achieve a more stable threshold voltage and subthreshold characteristics in the device, the electric field at the Schottky gate/p-GaN junction should be relaxed to suppress the electron trapping and defect generation via optimization of the gate-stack.

IV. Conclusion

In this article, we have demonstrated high-performance normally-OFF p-GaN gate HEMTs on Si with an ultrahigh V_{BR} and excellent BFOM. Meanwhile, low R_{ON}, high $I_{DS,max}$, large V_{th}, suppressed current collapse, and nearly ideal *SS* are also achieved in the device. Temperature-dependent forward gate stress measurements have shown stable device operation with minimal threshold voltage shift. The outstanding device performance reveals the great potential of the cost-effective p-GaN gate HEMTs on Si for beyond 600-V power applications.

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